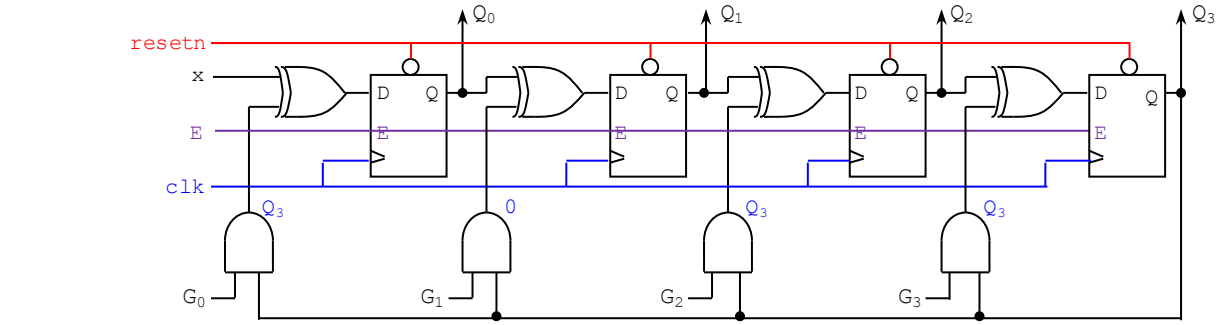
Solutions - Homework 4

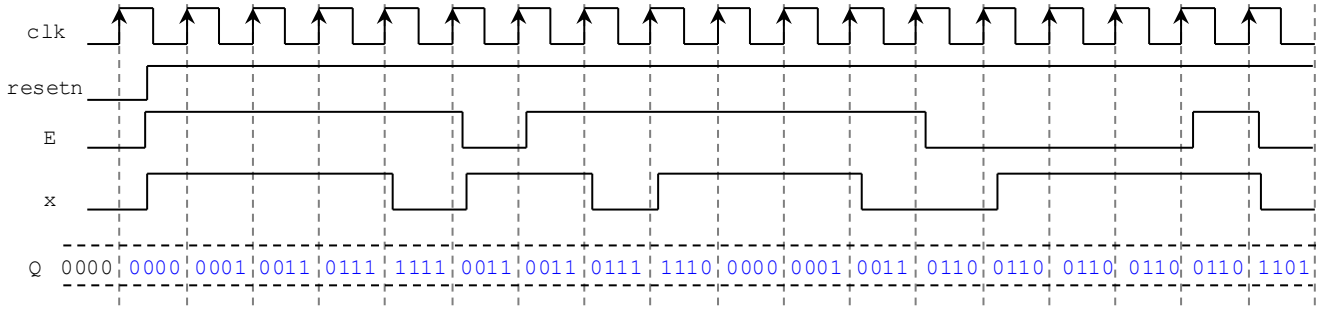
(Due date: April 1st @ 11:59 pm)

Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (13 PTS)

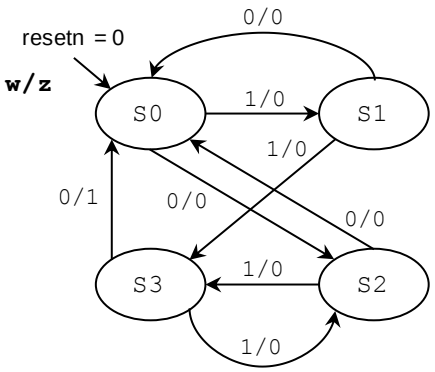
- Complete the timing diagram of the following circuit. $G = G_3G_2G_1G_0 = 1101$, $Q = Q_3Q_2Q_1Q_0$





PROBLEM 2 (20 PTS)

- Given the following State Machine Diagram: (10 pts)
  - ✓ Provide the State Table and the Excitation Table. (3 pts)
  - ✓ Get the excitation equations and the Boolean equation for z. (3 pts)
    Use S0 (Q=00), S1 (Q=01), S2 (Q=10), S3 (Q=11) to encode the states.
  - ✓ Sketch the Finite State Machine circuit. (3 pts)



PRESENT STATE			NEXTSTATE		
w	Q_1	Q_0 (t)	Q_1	Q_0 (t+1)	z
0	0	0	1	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	1
1	0	0	0	1	0
1	0	1	1	1	0
1	1	0	1	1	0
1	1	1	1	0	0

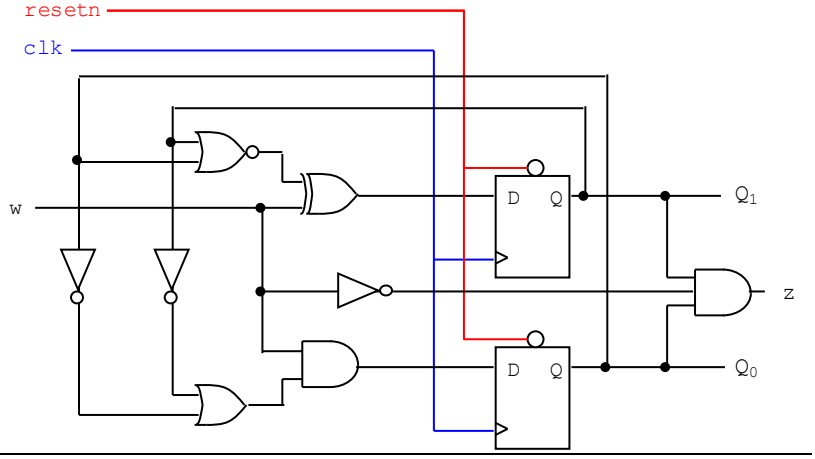
w	PRESENT STATE	NEXT STATE	z
0	S0	S2	0
0	S1	S0	0
0	S2	S0	0
0	S3	S0	1
1	S0	S1	0
1	S1	S3	0
1	S2	S3	0
1	S3	S2	0

$Q_1(t+1) \leftarrow \overline{(Q_1 + Q_0) \oplus w}$
$Q_0(t+1) \leftarrow \overline{Q_1 Q_0} w$
$z = \bar{w} Q_1 Q_0$

State Assignment:
S0: Q=00 S1: Q=01
S2: Q=10 S3: Q=11

- ✓ Is it a Mealy or Moore Machine?

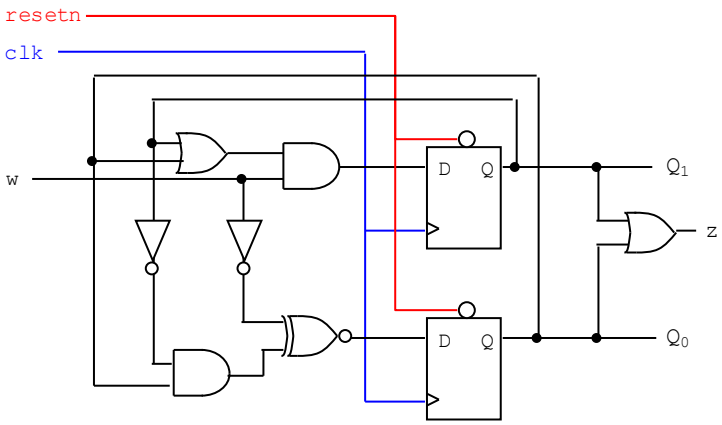
This is a Mealy FSM



- Provide the State Diagram (any representation), the Excitation Table, and the Excitation equations of the following Finite State Machine: (10 pts)

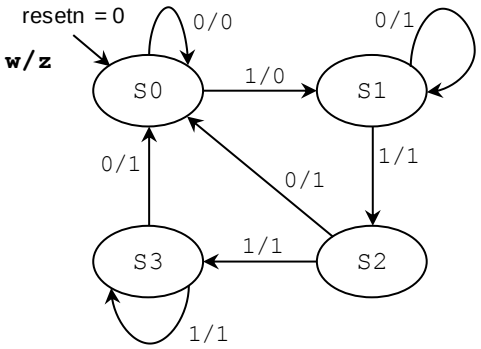
$Q_1(t+1) \leftarrow (Q_1 + Q_0)w$
$Q_0(t+1) \leftarrow (\overline{Q_1}Q_0) \oplus w$
$z = Q_1 + Q_0$

State Assignment:
S0: Q = 00
S1: Q = 01
S2: Q = 10
S3: Q = 11



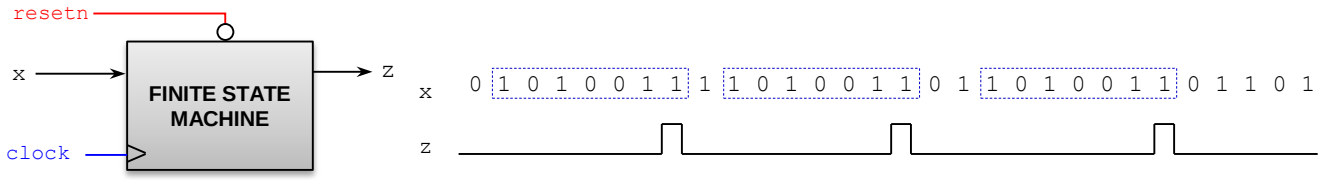
PRESENT STATE			NEXTSTATE		
w	Q_1	Q_0 (t)	Q_1	Q_0 (t+1)	z
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	0	1
0	1	1	0	0	1
1	0	0	0	1	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	1

w	PRESENT STATE	NEXT STATE	z
0	S0	S0	0
0	S1	S1	1
0	S2	S0	1
0	S3	S0	1
1	S0	S1	0
1	S1	S2	1
1	S2	S3	1
1	S3	S3	1



PROBLEM 3 (21 PTS)

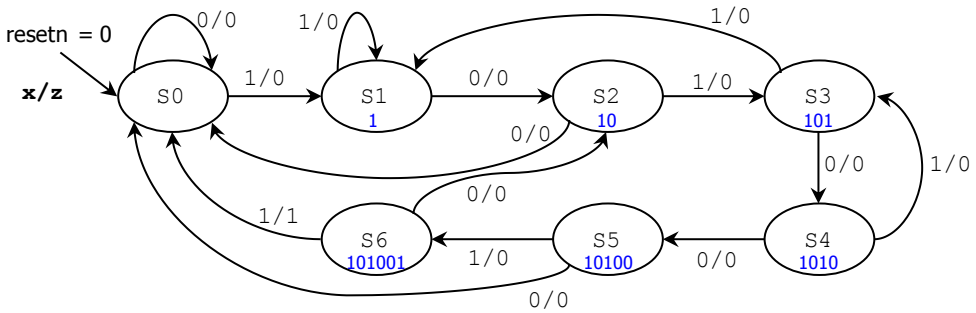
- Sequence detector: The machine generates $z = 1$ when it detects the sequence 1010011. Once the sequence is detected, the circuit looks for a new sequence.



- Draw the State Diagram (any representation), State Table, and the Excitation Table of this circuit with input x and output z. (14 pts)
- Provide the excitation equations and the Boolean equation for z (simplify your circuit: K-maps or Quine-McCluskey).
- Sketch the circuit. Is this a Mealy or a Moore machine? Why? (3 pts)

- *State Diagram, State Table, and Excitation Table*:

State Assignment:
S0: Q=000 S1: Q=001
S2: Q=010 S3: Q=011
S4: Q=100 S5: Q=101
S6: Q=110



This a Mealy Machine. The output 'z' depends on the input as well as on the present state.

x	PRESENT STATE	NEXT STATE	z
0	S0	S0	0
0	S1	S2	0
0	S2	S0	0
0	S3	S4	0
0	S4	S5	0
0	S5	S0	0
0	S6	S2	0
1	S0	S1	0
1	S1	S1	0
1	S2	S3	0
1	S3	S1	0
1	S4	S3	0
1	S5	S6	0
1	S6	S0	1

	PRESENT STATE	NEXTSTATE	
x	$Q_2Q_1Q_0$ (t)	$Q_2Q_1Q_0$ (t+1)	z
0	0 0 0	0 0 0	0
0	0 0 1	0 1 0	0
0	0 1 0	0 0 0	0
0	0 1 1	1 0 0	0
0	1 0 0	1 0 1	0
0	1 0 1	0 0 0	0
0	1 1 0	0 1 0	0
0	1 1 1	X X X	X
1	0 0 0	0 0 1	0
1	0 0 1	0 0 1	0
1	0 1 0	0 1 1	0
1	0 1 1	0 0 1	0
1	1 0 0	0 1 1	0
1	1 0 1	1 1 0	0
1	1 1 0	0 0 0	1
1	1 1 1	X X X	X

- *Excitation equations, minimization, and circuit implementation:*

$Q_2(t+1) = \bar{x}Q_2\overline{Q_1}\,\overline{Q_0} + xQ_2Q_0 + \bar{x}Q_1Q_0$
$Q_1(t+1) = \bar{x}\overline{Q_2}\,\overline{Q_1}Q_0 + x\overline{Q_2}Q_1\overline{Q_0} + xQ_2\overline{Q_1} + \bar{x}Q_2Q_1 = \bar{x}\overline{Q_2}\,\overline{Q_1}Q_0 + x\overline{Q_2}Q_1\overline{Q_0} + Q_2(x \oplus Q_1)$
$Q_0(t+1) = Q_2\overline{Q_1}\,\overline{Q_0} + x\overline{Q_2}$

$z = xQ_2Q_1$

$Q_2(t+1)$

Q_1Q_0 \ xQ_2	00	01	11	10
00	0	1	0	0
01	0	0	1	0
11	1	X	X	0
10	0	0	0	0

$Q_1(t+1)$

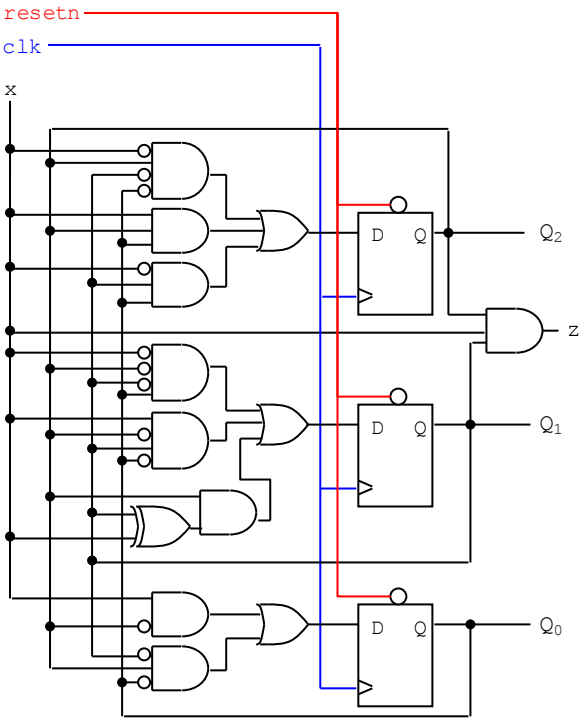
Q_1Q_0 \ xQ_2	00	01	11	10
00	0	0	1	0
01	1	0	1	0
11	0	X	X	0
10	0	1	0	1

$Q_0(t+1)$

Q_1Q_0 \ xQ_2	00	01	11	10
00	0	1	1	1
01	0	0	0	1
11	0	X	X	1
10	0	0	0	1

z

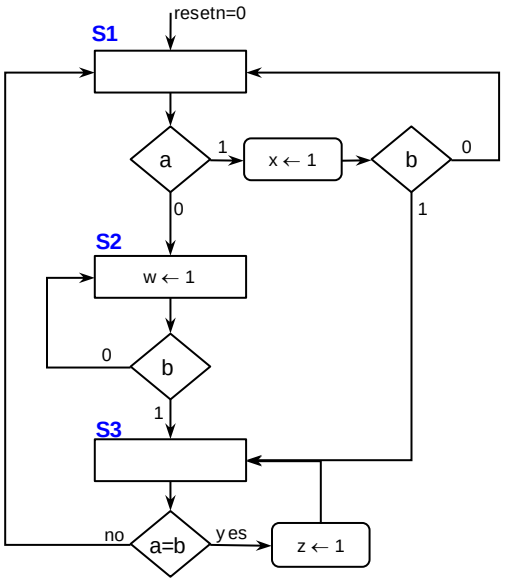
Q_1Q_0 \ xQ_2	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	X	X	0
10	0	0	1	0



PROBLEM 4 (14 PTS)

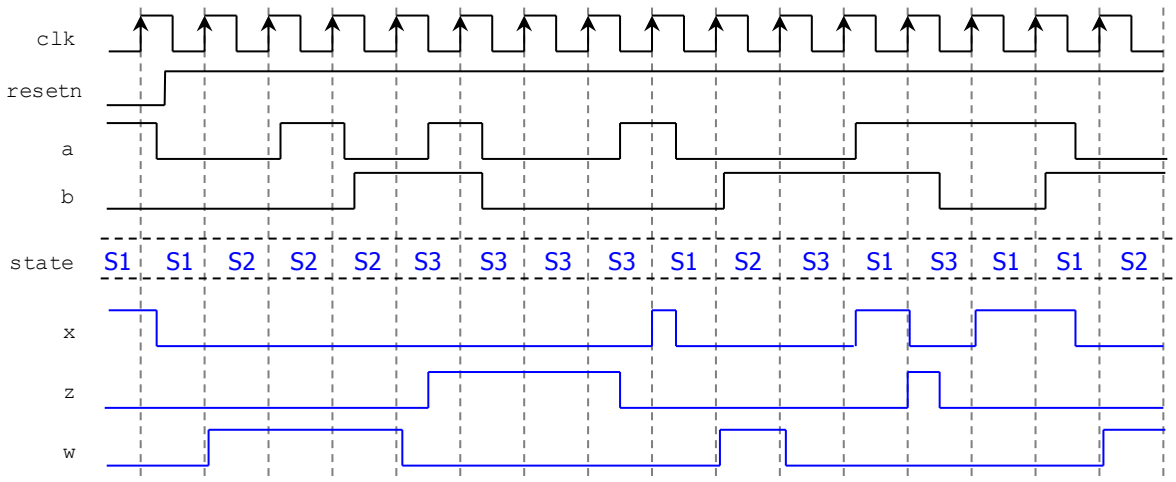
- Draw the State Diagram (in ASM form) of the FSM whose VHDL description is shown below. Is it a Mealy or a Moore FSM?
- Complete the Timing Diagram.

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
   port ( clk, resetn: in std_logic;
          a, b: in std_logic;
          x,w,z: out std_logic);
end circ;
```



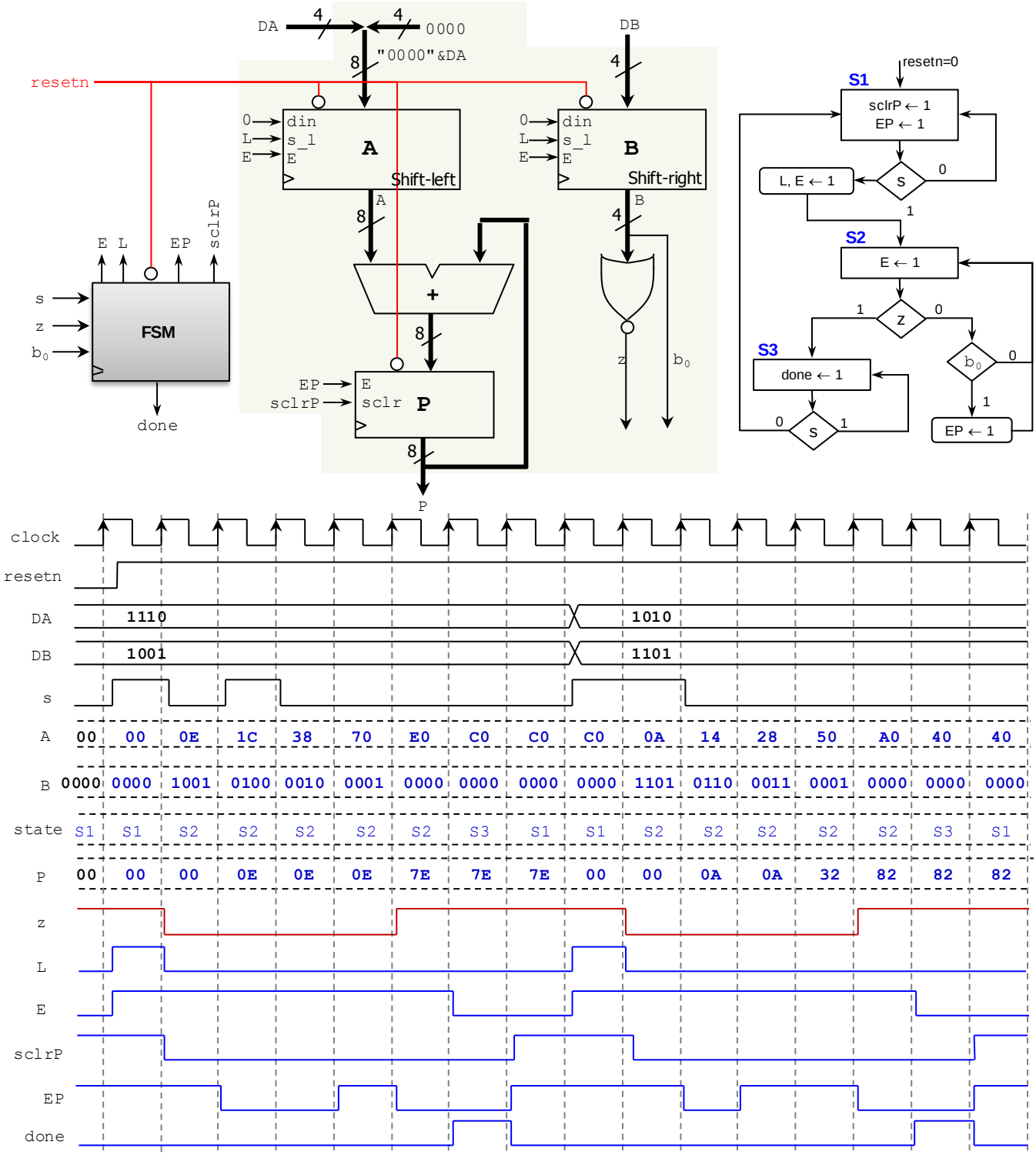

```
architecture behavioral of circ is
   type state is (S1, S2, S3);
   signal y: state;
begin
  Transitions: process (resetn, clk, a, b)
  begin
     if resetn = '0' then y <= S1;
     elsif (clk'event and clk = '1') then
        case y is
          when S1 =>
            if a = '1' then
              if b = '1' then y <= S3; else y <= S1; end if;
            else
              y <= S2;
            end if;

          when S2 =>
            if b = '1' then y <= S3; else y <= S2; end if;

          when S3 =>
            if a = b then y <= S3; else y <= S1; end if;
        end case;
     end if;
  end process;

  Outputs: process (y, a, b)
  begin
      x <= '0'; w <= '0'; z <= '0';
      case y is
         when S1 => if a = '1' then x <= '1'; end if;
         when S2 => w <= '1';
         when S3 => if a = b then z <= '1'; end if;
      end case;
  end process;
end behavioral;
```

This a Mealy Machine. The outputs depend on the input as well as on the present state.



PROBLEM 5 (17 PTS)

- Complete the following timing diagram (`A` and `P` are specified as hexadecimals) of the following Iterative unsigned multiplier. The circuit includes an FSM (in ASM form) and a datapath circuit.
- Refer to the Lecture Notes for more details of the behavior of the generic components:
  - ✓ Register (for `P`): *sclr*: synchronous clear. Here, if $E = sclr = 1$, the register contents are initialized to 0.
  - ✓ Parallel access shift registers (for `A` and `B`): If $E = 1$: $s\_l = 1 \rightarrow$ Load, $s\_l = 0 \rightarrow$ Shift



PROBLEM 6 (15 PTS)

- Attach a printout of your Project Status Report (no more than 3 pages, single-spaced, 2 columns). This report should contain the current status of the project, including more details about the design and its components. You **MUST** use the provided template (`Final Project - Report Template.docx`).